Thermal Oxide Grown on High Index Silicon Wafers.

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Summary

Even though the MOS technology was developed originally on the (0 0 1)-Si surface, some studies have shown that several MOS parameters can be optimized using other silicon orientations [1-3]. (1 1 4) and (5 5 12) Si surfaces presents a periodical surface roughness that may have technological applications [4]; however, the oxide grown on these surface orientations has not been studied. In this work we investigate the behavior of the oxide thickness in high index Si and compare it to oxides grown on standard surface orientations.

Experimental

Using (0 0 1), (1 1 1) and (1 1 0)-Si as references, we characterized the thermal oxide thickness grown on (1 1 4) and (5 5 12)-Si for 4 fabrication processes. Table I shows the details of such processes.

Table I. Orientation, gate material, type, and number of wafers used in the fabrication processes (**A-D**).

	(0 0 1)	(1 1 4)	(5 5 12)	(1 1 1)	(1 1 0)	Gate
A	2, n	2, n	4, n	-	-	Poly
B	2, n	2, n	2,n. 2,p	-	-	Poly
C	1, n	1, n	1, n	1, n	1, p	Al
D	1, n	1, n	1, n	1, n	1, p	Al

A was a standard CMOS process, **B** was a p-well MOS-process, whereas **C** and **D** were just MOS capacitors processes. We designed the process in order to obtain a gate oxide thickness in (0 0 1) of ~600Å for **A**, **B** and **C;** for **D** process the thickness was ~150Å.

Results

The oxide thickness was obtained from the maximum capacitance of C-V measurements, results are shown in Figs. 1-4. In the **A**, **B** and **C** processes, we obtained the average of all the thicknesses, and normalized to the thickness in (0 0 1):

1 : 1.094 : 1.155 : 1.161 : 1.192

In terms of the orientations, the order of the thickness is:

(0 0 1) < (1 1 4) < (5 5 12) < (1 1 0) < (1 1 1)

For the **D** process (thinner oxide), the thickness relationship maintained the same order in orientation, and the values normalized to (0 0 1) were:

1 : 1.172 : 1.315 : 1.456 : 1.576

Further details on the fabrication process and discussion of the results will be presented at the time of the conference.

Acknowledgments

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References

[1] M. Aoki, K, Yano, T. Masuhara, S, Ikeda and S. Meguro, *IEEE Transactions on Electron Devices*, **ED-34 No. 1**, 52 (1987).
[2]M. Aoki, K, Yano, T. Masuhara, and K. Shimohigashi, *IEEE Transactions on Electron Devices*, **ED-36, No. 8**, 1429 (1989).
[3]H.-J. Müssig, J. Dabrowits, S. Hinrich, *Solid State Electronics*, **45**, 1219 (2001).
[4] D. L. Kendall and M. Kendall, *NSTI-Nanotech 2004*, **3**, p. 510 (2004).

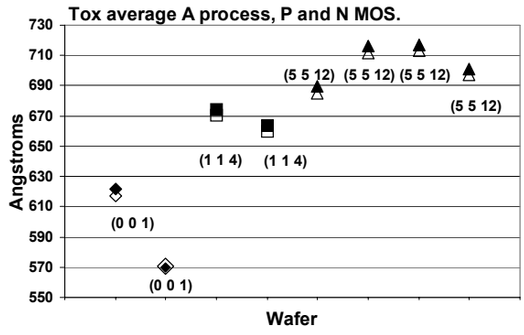

Figure 1. Oxide thicknesses obtained in process **A**. Filled symbols stand for p-MOS, and empty symbols for n-MOS capacitors.

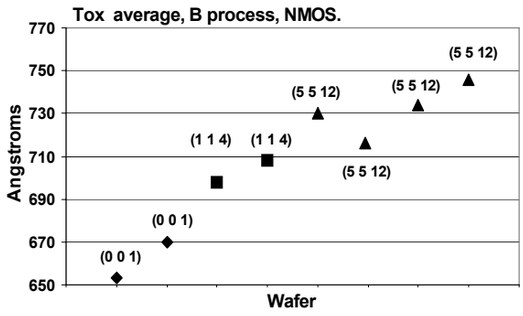

Figure 2. Oxide thicknesses obtained for **B** process.

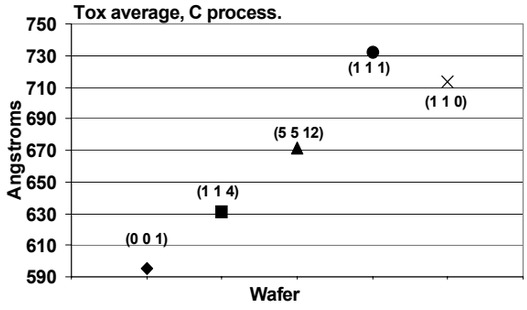

Figure 3. Oxide thicknesses obtained for **C** process.

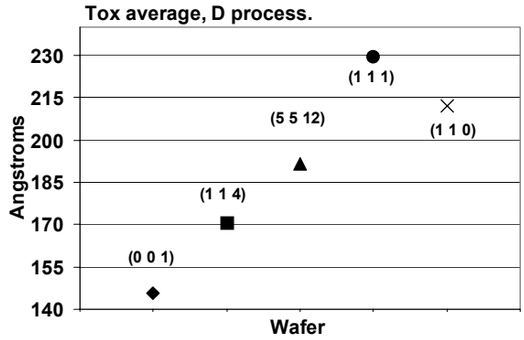

Figure 4. Oxide thicknesses obtained for **D** process.